REMARKS

Claims 1-11, 24-29, and 32-45 are pending in the present application. Claims 12-23, 30, 31, and 46-60 have been cancelled without prejudice or disclaimer to the subject matter contained therein. The Applicants reserve the right to file divisional applications directed to this cancelled subject matter. Claims 1-11, 24, 25, and 32-45 have been withdrawn from consideration as being drawn to a non-elected species. The Applicants respectfully submit that Claims 1-11, 24, 25, and 32-45 should be entitled to consideration because, for the reasons set forth below, generic claim 26 is allowable over the prior art of record and each of these claims to the alleged additional species are written in dependent form and/or include all the limitations of allowable generic claim 26.

As set forth above, the claims have been amended to enhance the particularity and distinctness of the language used to claim the subject matter which the Applicants regard as their invention.

I. ARGUMENTS

A. Rejection under 35 U.S.C. §102(e)

Claims 26 and 28 have been rejected under 35 U.S.C. §102(e) as being anticipated by Nakabayashi (US-A-6,215,194). This rejection under 35 U.S.C. §102(e) is respectfully traversed.

The presently claimed invention, as set forth in amended independent claim 26, is directed to a method for protecting a MEMS wafer during a dicing. The claimed method mounts, upon a backside of the MEMS wafer, a layer of dicing tape, the MEMS wafer having a plurality of MEMS structure sites on a front side and a plurality of through holes, each through hole corresponding to a MEMS structure site, the through holes being formed such that each through hole penetrates through the wafer from the backside of the wafer to the front side; dices the MEMS wafer into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole; and mounts, upon the dicing tape, a layer of transfer tape.

The Examiner, in formulating the present rejection under 35 U.S.C. §102(e), alleges that Nakabayashi anticipates the presently claimed invention. More specifically, the Examiner

alleges that Nakabayashi teaches mounting, upon a backside of a wafer (1), a layer of dicing tape (2), the wafer having a front patterned side and a plurality of etched ports (41 or 42) on a backside, the etched ports providing a possible leak path from a backside of the wafer to the front patterned side of the wafer; dicing the wafer into a plurality of dies; and mounting, upon the diced layer of dicing tape, a layer of transfer tape (43). The Applicants respectfully traverse these allegations.

As set forth above, amended independent claim 26 sets forth that upon a backside of the MEMS wafer, a layer of dicing tape is mounted wherein the MEMS wafer has a plurality of MEMS structure sites on a front side and a plurality of corresponding through holes, each through hole corresponding to a MEMS structure site. Amended independent claim 26 further states that the through holes are formed such that each through hole penetrates through the wafer from the backside of the wafer to the front side. Moreover, amended independent claim 26 sets forth that the MEMS wafer is diced into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole. Lastly, amended independent claim 26 sets forth that a layer of transfer tape is mounted upon the dicing tape.

In contrast, Nakabayashi teaches a dicing method wherein a wafer (1) has formed thereon a wafer sheet (2) having a thermosetting adhesive layer (43) on each side. Moreover, Nakabayashi teaches that the wafer is diced to form separation grooves (42), which surround the semiconductor element (3) to enable the die having the semiconductor element (3) to be separated from the wafer.

Nakabayashi fails to teach that a layer of dicing tape is mounted wherein the MEMS wafer has a plurality of MEMS structure sites on a front side and a plurality of corresponding through holes wherein each through hole corresponds to a MEMS structure site because the separation grooves (42) of Nakabayashi are a result of the dicing operation, not a structure already present upon the wafer before dicing. Furthermore, Nakabayashi fails to teach that the MEMS wafer is diced into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole because dicing of Nakabayashi results in a plurality of semiconductor elements with no corresponding through holes. Lastly, Nakabayashi fails to teach that a layer of transfer tape is mounted upon the dicing tape because Nakabayashi, at best,

teaches that the wafer sheet (2) may function as a dicing tape, but is void of any teaching of an additional tape layer being mounted thereon.

Therefore, contrary to the Examiner's conclusion, Nakabayashi fails to anticipate the presently claimed invention, as set forth by amended independent claim 26.

Accordingly, in view of the amendments and reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection under 35 U.S.C. §102(e).

B. Rejection under 35 U.S.C. §103

Claims 26-28 have been rejected under 35 U.S.C. §103 as being unpatentable over Yonezawa (JP55-102254) in view of Smith (US-A-5,622,900). This rejection under 35 U.S.C. §103 is respectfully traversed.

The presently claimed invention, as set forth in amended independent claim 26, is directed to a method for protecting a MEMS wafer during a dicing. The claimed method mounts, upon a backside of the MEMS wafer, a layer of dicing tape, the MEMS wafer having a plurality of MEMS structure sites on a front side and a plurality of through holes, each through hole corresponding to a MEMS structure site, the through holes being formed such that each through hole penetrates through the wafer from the backside of the wafer to the front side; dices the MEMS wafer into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole; and mounts, upon the dicing tape, a layer of transfer tape.

The Examiner, in formulating the present rejection under 35 U.S.C. §103, alleges that Yonezawa teaches the presently claimed invention except for the application of a transfer tape layer to the dicing tape. To meet this deficiency in Yonezawa, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to combine Yonezawa with the teachings of Smith, which allegedly teaches the application of a transfer tape to a dicing tape, to meet all the limitations of the presently claimed invention. The Applicants respectfully traverse these allegations.

As set forth above, amended independent claim 26 sets forth that upon a backside of the MEMS wafer, a layer of dicing tape is mounted wherein the MEMS wafer has a plurality of MEMS structure sites on a front side and a plurality of corresponding through holes, each through hole corresponding to a MEMS structure site. Amended independent claim 26 further

states that the through holes are formed such that each through hole penetrates through the wafer from the backside of the wafer to the front side. Moreover, amended independent claim 26 sets forth that the MEMS wafer is diced into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole. Lastly, amended independent claim 26 sets forth that a layer of transfer tape is mounted upon the dicing tape.

On the other hand, Yonezawa and Smith, singly or in combination, teach a dicing method wherein a wafer has formed thereon a dicing tape. Moreover, Smith, singly, teaches an additional tape mounted upon the dicing tape.

However, Yonezawa and Smith, singly or in combination, fail to teach that a layer of dicing tape is mounted wherein the MEMS wafer has a plurality of MEMS structure sites on a front side and a plurality of corresponding through holes wherein each through hole corresponds to a MEMS structure site because the grooves (23) of Yonezawa are a result of the dicing operation, not a structure already present upon the wafer before dicing; the groves (20) of Yonezawa are merely indentations, not a through hole which penetrates through the wafer from the backside of the wafer to the front side; and/or Smith is void of any teachings suggesting through holes.

Furthermore, Yonezawa and Smith, singly or in combination, fail to teach that the MEMS wafer is diced into a plurality of dies such that each die includes a MEMS structure site and a corresponding through hole because dicing of both Nakabayashi and Smith, singly or in combination, result in a plurality of semiconductor elements with no corresponding through holes.

Therefore, contrary to the Examiner's conclusion, the alleged combination of Yonezawa and Smith fails to teach, suggest, or render obvious the presently claimed invention, as set forth by amended independent claim 26.

Accordingly, in view of the amendments and reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection under 35 U.S.C. §103.

C. Rejection under 35 U.S.C. §103

Claim 29 has been rejected under 35 U.S.C. §103 as being unpatentable over Yonezawa (JP55-102254) in view of Smith (US-A-5,622,900) and Ohkawa et al. (US-A-5,360,873). This rejection under 35 U.S.C. §103 is respectfully traversed.

With respect to dependent claim 29, the Applicants, for the sake of brevity, will not address the reasons supporting patentability for this individual dependent claim, as this claim depends directly from the allowable independent claim 26 for the reasons set forth above. The Applicants reserve the right to address the patentability of this dependent claim at a later time, should it be necessary.

Accordingly, in view of the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejection under 35 U.S.C. §103.

D. Rejection under Obviousness-type Double-patenting

Claims 26-29 have been provisionally rejected under the doctrine of obviousness-type double-patenting over claims 115 and 117 of co-pending patent application number 10/006,966 in view of Smith (US-A-5,622,900). This rejection under the doctrine of obviousness-type double-patenting is respectfully traversed.

The Applicants respectfully that this provisional rejection be held in abeyance until the final allowable language of claims 115 and 117 of co-pending patent application number 10/006,966.

Accordingly, in view of the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the present provisional rejection under the doctrine of obviousness-type double-patenting.

II. CONCLUSION

Accordingly, in view of all the reasons set forth above, the Examiner is respectfully requested to reconsider and withdraw the present rejections. Also, an early indication of allowability is earnestly solicited.

Respectfully submitted,

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